ABSTRACT OF THE DISCLOSURE

A high performance differential delay circuit for is revealed. The delay unit may be used in a variety of circuits requiring delay units, including voltage-controlled oscillators, voltage controlled delay lines, delay locked loops, phase accumulators, phase locked loops, and direct frequency syntheses. The circuit is desirably manufactured at one time with CMOS technology, and is therefore relatively immune to temperature changes, manufacturing process variations, input voltage fluctuations, and frequency ranges. The circuit achieves its goals by using a minimum number of transistors, and takes advantage of CMOS manufacturing techniques by balancing the NMOS and PMOS transistors used.